First International Conference on Semiconductor Materials packaging, AI&ML, Reconfigurable VLSI Architectures for IoT, Future Communication Technologies (SMART-2024)

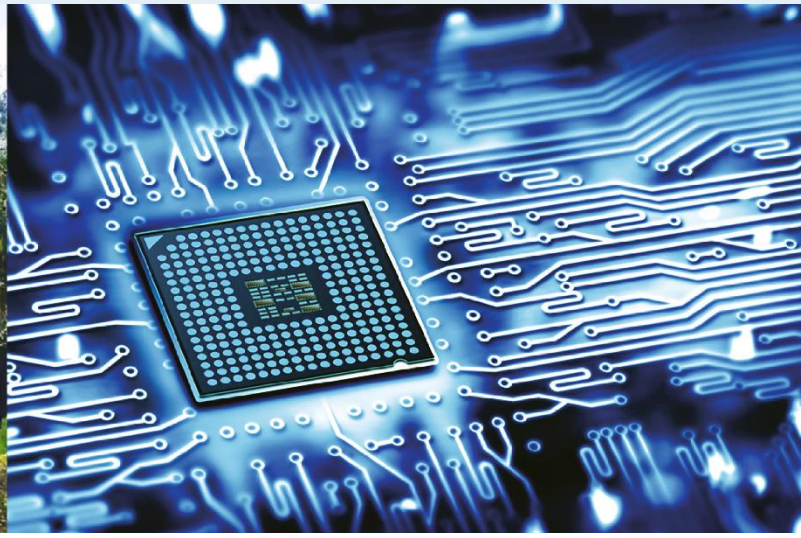
Conference Dates: 19 - 20 September 2024

B V RAJU INSTITUTE OF TECHNOLOGY

Department of Electronics and Communication Engineering

Vishnupur, Narsapur, Medak District, Telangana

http://smart2024.bvrit.ac.in/



About the Conference

The International Conference on Semiconductor Materials Packaging, AI&ML, Reconfigurable VLSI architectures based IoT, Future Communication Technologies **(SMART-2024)** is aligned with the targets of **India Semiconductor Mission (ISM)** to provide a platform for researchers, academicians, industry experts, and practitioners to exchange ideas, present research findings, and discuss emerging trends and challenges in the specified fields. **SMART-2024** seeks to foster collaboration, innovation, and knowledge dissemination by bringing together experts and stakeholders from diverse backgrounds to address key Issues and explore new research directions. Key features of SMART-2024 include comprehensive coverage of topics, distinguished keynote speakers, paper presentations for scholarly discussions, specialized workshops and tutorials for hands-on learning, and ample networking opportunities for professional connections. The conference targets a diverse audience including researchers, academicians, scientists, engineers, technologists, industry professionals, students, policymakers, and other stakeholders interested in VLSI, IoT, AI-ML, communication systems, semiconductor packaging, hetero architecture devices, and Nano materials.

Conference Highlights:

- Keynote Talks
- Oral Presentation
- Online Presentation
- Poster Presentation
- Industry Exhibits

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Key Dates

Call for Papers	20th March 2024
Submission Deadline	31st Aug 2024
Acceptance Notification	01st Sept 2024
Early Bird Registration	5th Sept 2024

Registration

Academicians	INR 8,500
Students/ Research Scholars	INR 6,500
Industry Participants	INR 10,000
International Participants	USD 150

Conference Tracks

- VLSI & IoT
- Communication
- Devices & circuits
- Semiconductor Packaging
- AI & ML
- Nano Materials

About the Institute

B V Raju Institute of Technology (BVRIT) was established by the eminent philanthropist (Late) Padmabhushan Dr. B.V. Raju under the aegis of Sri Vishnu Educational Society (SVES) in the year 1997. BVRIT was granted UGC – Autonomous Status from the year 2014. The Institute is also duly approved by the AICTE and the Government of Telangana State and is affiliated to JNTU, HYDERABAD. CSE, IT, ECE, EEE, Chemical, Mechanical, and Civil Engineering branches in BVRIT are accredited by NBA. BVRIT is accredited by NAAC with an A+ grade.

This institution is also looked after by a body of distinguished professionals from IITs, engineering and government sectors, led by Sri K. V. Vishnu Raju garu. He is a graduate in Chemical Engineering from REC, Trichy and a postgraduate from Michigan Technological University, USA. The purpose of establishing BVRIT was to provide quality technical education in a perfect ambiance for the all-round development of a student. Under the hegemony of our Chairman, Sri K. V. Vishnu Raju, BVRIT made a quantum leap in its reputation for its best teaching-learning practices, high-quality intake, excellent infrastructure facilities, the highest number of placements, etc.

About the Department

Department of ECE, BVRIT was established in the year 1999 with the motive of imparting state-of the-art and facilitating quality education, training, and research in the field of Electronics and Communication Engineering and allied areas. The Department is well equipped with sophisticated special laboratories in the areas of embedded systems, Digital Signal Processing, VLSI design, Robotics, Advanced Communications and Artificial Intelligence, and Machine Learning. Conduction of skill development programs and industry-supported training/workshops in the Department has broadened the opportunities for students and professionals to develop core subject knowledge which is duly complemented by leadership training interventions, thereby helping the students to make a mark in the global arena.

The department is laser-focused on students to submit innovative ideas to premier national and international technical contests such as the STM Innovation Challenge, Smart India Hackathon, TI Design Contest, Rural Innovators Startup Conclave, Altair Global Contest, and HackwithInfy. The department is very keen on formulating the curriculum in line with the promoted technical skill set referring to the industry needs and also aligning with the policy-making of governing and private bodies such as AICTE, UGC, NASSCOM, Eduskills and ISM.

TRACK 01 — VLSI & IoT:

- Ultra-Low Power VLSI Design for IoT Devices
- Integration of IoT Sensors and Actuators in VLSI Systems
- Energy-Efficient Circuit Design for IoT Applications
- IoT Edge Computing and VLSI Implementations
- Security and Privacy in VLSI-based IoT Systems
- Custom ASIC Designs for IoT Sensor Nodes
- VLSI-IoT Devices Energy Harvesting Techniques
- Embedded ML and AI for IoT on VLSI Chips.

TRACK 02 — Semiconductor Packaging:

- Advanced VLSI Packaging Technologies
- 3D Integrated Circuit Packaging
- System-in-Package (SiP) Design and Integration
- Fan-Out Wafer Level Packaging (FOWLP)
- Flip-chip and Chip-on-Board Packaging
- Interconnects and Micro-bumps for VLSI Packaging
- Wafer-Level Chip Scale Packaging (WLCSP)
- Thermal Management in VLSI Packaging
- Electrical and Mechanical Reliability of VLSI Packages
- Wire Bonding and Die Attach Techniques
- VLSI Packaging Materials and Substrates

TRACK 03 — Communication:

- 5G and 6G Standardization and Roadmaps
- Massive MIMO and Beam forming in 5G & 6G Systems
- Ultra-Reliable Low Latency Communications in 5G & 6G
- Edge Computing and Mobile Edge Computing in 5G & 6G
- Wireless Network Resilience and Reliability for 5G & 6G
- Satellite Integration and Space-based Communications
- 6G Use Cases and Beyond Future Applications and Services.

TRACK 04 — AI & ML:

- Multi-Chip Module (MCM) Packaging AIML & VLSI:
- AI/ML Hardware Accelerators for VLSI Systems
- Neuromorphic Computing and VLSI Implementation
- Edge Computing & VLSI Integration for AI Applications
- Hardware Machine Learning Algorithms for VLSI Design
- VLSI-based Deep Learning Accelerators
- Energy-efficient AI/ML Hardware Design for IoT Devices
- Reconfigurable Hardware Platforms for Data Science and ML
- Advanced developments in AI/ML applications
- Hardware Security for AI/ML Models in VLSI Systems

TRACK 05 — Devices & circuits:

- Compact device modeling for energy efficiency
- Quantum electronics, Ballistic transport mechanism
- Emerging devices & and characteristics (FINFETS, TFET)
- Beyond CMOS –III-V HEMT, Ga2o3 & UWB Semiconductor
- 2D, 3D Materials graphite, CNT-FETS & Nanotubes, SETs & spintronics.
- Flexible electronics & wearable devices
- Energy storage, High-efficiency solar cells
- Analog, digital, mixed-signal VLSI circuits
- System on chip, Bio electronics
- Reconfigurable circuits & optimizing techniques
- HDL-based FPGA design, testing, and verification

TRACK 06 — Nano Materials:

- Biomaterials & Bio sensing
- Materials for energy storage conversion
- Computational material science and modeling
- Surface engineering thin ·lm & coating
- Emerging materials and the latest technologies
- High Speed Materials for Photonics & Electronics
- Materials for green energy storage
- Materials for Sustainable Development

Keynote Speakers

Prof. Madhavan Swaminathan
Department Head of Electrical Engineering,
William E. Leonhard Professor
Penn State University, USA

Prof. Douglas Werner
School of Electrical Engineering and
Computer Science, Electrical Engineering
Penn State University, USA

Prof. Arun Chandrasekhar
Product design Engineer,
Intel Bangalore & Adjunct Faculty,
IISC Bangalore, India

Prof. S P Duttagupta
Associate Professor, Electrical Engineering
Indian Institute of Technology Bombay,
Mumbai, India

Prof. Yalagala Bhavani Prasad
Electronic & Nano scale Engineering
University of Glasgow, Glasgow City,
Scotland, United Kingdom

Prof. Asral Bahari Jambek
Head, Centre of Excellence in
Micro Systems Technology (MiCTEC)
University Malasia, Malaysia

Prof. Anil Kumar Vuppala
International Institute of
Information Technology (IIIT)
Gachibowli, Hyderabad, India

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and Computer Science
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Dr. N. Mohan Kumar. Professor, Dept. of ECE, B V Raju Institute of Technology, Narsapur, Medak dist., Telangana, India.

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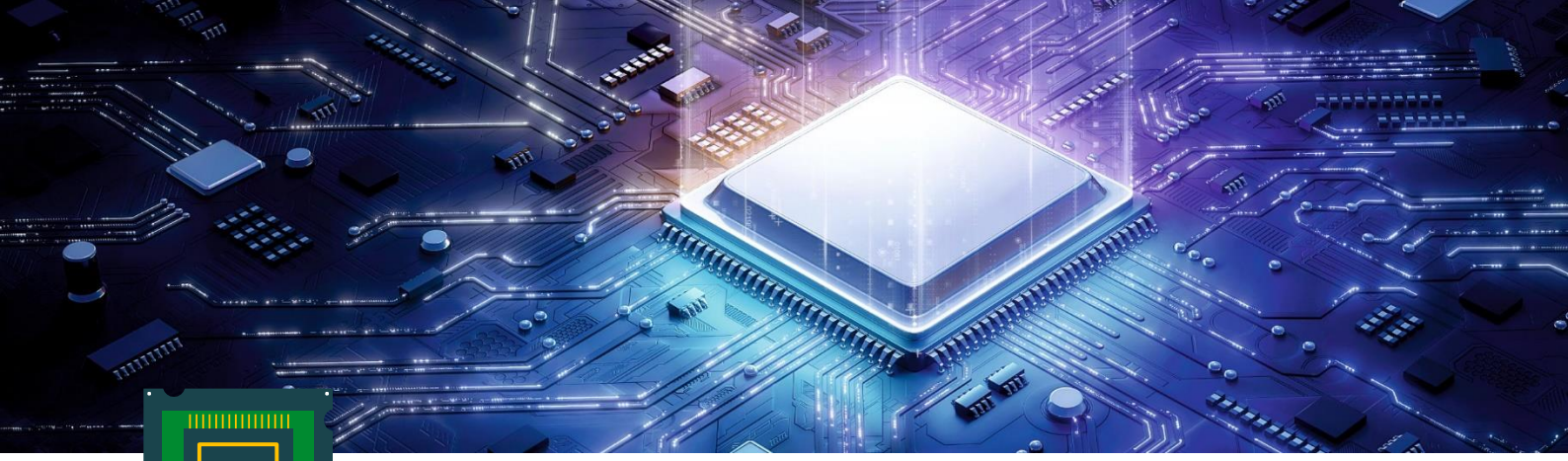

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The abstracts/extended abstracts must be submitted through Microsoft Conference Management Tool Kit (CMT). Each author confirms that he/she is aware of the publication ethics & malpractice statement and the privacy policy of the event. Next, every Submission will undergo peer review process by at least 2 reviewers and the decisions along with the reviewer comments will be communicated to the corresponding author in due course. The authors are expected to have significant contribution in the article and must meet the guidance of Taylor and Francis publications. The minimum paper length is 5 pages. Authors with more than 5 pages should pay INR 500 or 10 USD per page.

Paper format: Taylor & Francis
https://shorturl.at/ekqKW

Submission link:
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